UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,381	07/09/2003	Douglas Brisbin	NSC1-M2900 [P05632]	1278

7590 03/01/2005

STALLMAN & POLLOCK L.L.P.
Attn: Brian J. Keating
353 Sacramento Street
Suite 2200
San Francisco, CA 94111

EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,381	BRISBIN ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-10,12 and 13* is/are rejected.

7)☒ Claim(s) *2,7 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on December 10, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 4-6, 8-10, 12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art (hereinafter APA).

Regarding claim 1, Figures 1 and 2 of the instant application (which show the APA) disclose an LDMOS transistor array structure comprising: an array that includes a plurality of alternating source regions 122 and a plurality of alternating drain regions 120 formed in a semiconductor substrate to define a checkerboard pattern of said alternating source and drain regions, wherein at least a first source region (middle source region) of the alternating source regions includes a first source region face (top inside face) which is orientated toward a first drain region face (right side) of a first drain region (drain region to left of middle source region) of the plurality of alternating drain regions, and wherein the first drain region face has a drain region face length and the source region face has a source region face length, and wherein the drain region face length is greater than the source region face length; a conductive source region interconnect 146 structure formed in electrical contact with each of the plurality of alternating

source regions in the array to electrically connect said source regions in parallel; and a conductive drain region interconnect structure 144 formed in electrical contact with each of the plurality of alternating drain regions in the array to electrically connect said drain regions in parallel. Note that it is considered the source regions have four outside faces and four inside faces, wherein the inside faces are the sides that contact region 126. As stated above, the top inside face (as shown in Figure 1 of the APA) is oriented toward the bottom drain region. This broad interpretation is reasonable since there is nothing in the specification that indicates the term "face" must be limited to the outside portion of a source region.

Regarding claims 2, 6, and 10, Figure 2 of the APA discloses the drain region 120 face length (width of region 120) is at least 1.5 times greater than the source region face length (which is equivalent to the width of region 126).

Regarding claims 4, 8, and 12, Figure 2 of the APA discloses the source region 122 faces have a source region face depth, and the drain region faces have a drain region face depth, and the source region face depth and the drain region face depth are substantially equal in length.

Regarding claims 5 and 13, Figures 1 and 2 of the APA disclose each of the alternating source regions 122 has four source region faces (inside faces), and each of the source region faces has the same source region face length, and wherein each of the alternating drain regions 120 has four faces, and each of the drain region faces has the same drain region face length.

Regarding claim 9, Figures 1 and 2 of the APA disclose a high power transistor including: a source region 122 (middle region) which includes a first source region face (top inside face) wherein the source region face has a source region face length, wherein the source region is a contiguous region of first conductivity type; a first drain region 120 (region to the left

of middle source region) which includes a first drain region face (right side) wherein the first drain region face has a drain region face length; a second drain region 120 (region to the right of the middle source region) which includes a second drain region face (left side) wherein the second drain region face has the drain region face length; wherein the source region is the only source region disposed between the first drain region face and the second drain region face; a source contact 146 coupled with the source region; a drain contact 144 coupled with the first drain region and the second drain region; a channel region disposed between the source region and the first drain region face and a second channel between the source region and the second drain region face; wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the first drain region and the second drain region; and wherein the drain region face length is longer than the source region face length.

Claims 1 and 9 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamamoto (US Pat. 6,437,402).

Regarding claim 1, Figures 1A and 1B of Yamamoto disclose an LDMOS transistor array structure comprising: an array that includes a plurality of alternating source regions 13 and a plurality of alternating drain regions 14 formed in a semiconductor substrate (col. 1, lines 15-17) to define a checkerboard pattern of said alternating source and drain regions, wherein at least a first source region (middle source region in bottom row) of the alternating source regions includes a first source region face (upper right side) which is orientated toward a first drain region face (bottom side) of a first drain region (drain region to up and to the right of the source

region) of the plurality of alternating drain regions, and wherein the first drain region face has a drain region face length and the source region face has a source region face length, and wherein the drain region face length is greater than the source region face length; a conductive source region interconnect 16 structure formed in electrical contact with each of the plurality of alternating source regions in the array to electrically connect said source regions in parallel; and a conductive drain region interconnect structure 17 formed in electrical contact with each of the plurality of alternating drain regions in the array to electrically connect said drain regions in parallel.

Regarding claim 9, Figures 1A and 1B of Yamamoto disclose a high power transistor including: a source region 13 (middle region of bottom row) which includes a first source region face (upper right side) wherein the source region face has a source region face length, wherein the source region is a contiguous region of first conductivity type; a first drain region 14 (drain region to up and to the right of the source region) which includes a first drain region face (bottom side) wherein the first drain region face has a drain region face length; a second drain region 14 (drain region down and to the left of the source region) which includes a second drain region face (upper side) wherein the second drain region face has the drain region face length; wherein the source region is the only source region disposed between the first drain region face and the second drain region face; a source contact 16 coupled with the source region; a drain contact 17 coupled with the first drain region and the second drain region; a channel region disposed between the source region and the first drain region face and a second channel between the source region and the second drain region face; wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the first drain

region and the second drain region; and wherein the drain region face length is longer than the source region face length.

Allowable Subject Matter

Claims 3, 7, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including the drain region face length is at least twice as long as the source region face length.

Response to Arguments

Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau
Examiner

February 24, 2005